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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	12

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,010	OLARIG ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to Application No. 10,039,010 filed on December 31, 2001. Claims 1-31 are pending in this application.

Status of claims

2. Claims 1-31 are presented for examination.

Claims 1-31 are rejected.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The oath is missing the inventors' signature.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23, and 25-31 are rejected under 35 U.S.C 102(e) as being unpatentable over Leung et al. (US 6,272,577).

As per claim 1, Leung et al. discloses a method for transacting between an initiator device and a plurality of target devices [*a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65]; configuring the plurality of target devices to associate a portion of memory with a particular target device of the plurality of target devices [*a memory device which is organized into small memory arrays, wherein only one array is activated for each normal memory access*; col.3, lines 54-56]; sending a multicast transaction from the initiator device to the plurality of target devices [*a memory device in accordance with the present invention provides multiple commands, one after another, to different arrays*; col.25, lines 15-17]; executing the transaction when the transaction is received by the plurality of target devices according to the configuration of the target device [*since each memory module is a complete functional unit, the memory module architectures allows parallel processes and multiple memory module operations to be performed within different memory modules*; col.4, lines 42-45].

As per claim 2, Leung et al. discloses assigning a base memory address to be shared by the plurality of target devices [*a base address which identifies the memory module*; col.10, lines 20-23; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65]; and assigning a first portion of memory

to a first target device of the plurality of target devices [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract].

As per claim 3, Leung et al. discloses the transaction is a read request for a block of stored data from memory [*a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *the address information comprises a base address of the memory device to be accessed*; col.31, lines 12-14]; reading the base memory address from the read request *[each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract *; the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; col.4, lines 31-33]; initiating a read operation by the plurality of target devices assigned to the base memory address [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *a base address which identifies the memory module*; col.10, lines 20-23]; fetching stored data from a portion of memory associated with each of the target devices, the data being concurrently fetched by each associated target device and sending the fetched data to the initiator device [*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 4, Leung et al. discloses, the transaction is a write request for data to be stored in memory [*a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27]; reading the base memory address from the write request [*address information comprises a base address of the memory device to be accessed*; col.31, lines 13-14; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27]; initiating a write operation by the plurality of target devices assigned to the base memory address [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract; *a base address which identifies the memory module*; col.10, lines 20-23]; and writing data of the write request to a portion of memory associated with each target device, the data being concurrently written by each associated target device[*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 5, Leung et al. discloses, wherein the target devices comprise input/output Controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 6, Leung et al. discloses, the target devices comprise disk array controllers [Fig. 19; *controller 1920*].

As per claim 7, Leung et al. discloses, the plurality of target devices comprise a target group, the target group addressable with a single base memory address [*the*

present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 8, Leung et al. discloses, a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 9, Leung et al. discloses, a method for transacting data stored in memory between an initiator device and detecting a multicast transaction request [*multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; accessing a first portion of memory by a first target device associated with the first portion of memory in response to the multicast transaction request [*when a memory read or write command is decoded, each memory module examines the communication ID of the command. All modules, except the module to which the command is addressed, go into an idle state until the read or write transaction is finished*; col.19, lines 42-47]; accessing a second portion of memory by a second target device associated with the second portion of memory concurrently with access to the first portion of memory in response to the multicast transaction request [*a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module*. col.10, lines 21-25].

As per claim 10, Leung et al. discloses, the target devices comprise input/output Contlollers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 11, Leung et al. discloses, the target devices comprise disk array Controllers [Fig. 19; *controller 1920*].

As per claim 12, Leung et al. discloses, wherein the first target device and the second target device are configured as part of a target group, the target group addressable with a single base memory address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 13, Leung et al. discloses, wherein a plurality of target devices are configured into multiple target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 14, Leung et al. discloses, multicast transaction is a multicast read

request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 15, Leung et al. discloses, wherein the multicast transaction is a multicast write request [*multiple bank operations such as broadcast-write and interleaved-access*; col.5, lines 27-29; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

As per claim 16, Leung et al. discloses, a computer system for communicating between an initiator device and multiple target devices comprising [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; a communication bus [*memory device and allowing each memory module to have a communication address on the I/O bus system*; col.4, lines 54-56]; an initiator device coupled to the communications bus for initiating a transaction request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46]; and a plurality of target devices coupled to the communications for executing the transaction request, the plurality of target devices executing the transaction request by each target device concurrently responding to a portion of the transaction request [*a first field contains a base address which identifies the memory module by*

communication address. A second field contains an address which identifies the memory array within the memory module. col.10, lines 21-25; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65; *a memory device in accordance with the present invention provides multiple commands, one after another, to different arrays*; col.25, lines 15-17].

As per claim 17, Leung et al. discloses the target device comprises input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 18, Leung et al. discloses a target device comprises disk array controllers [Fig. 19; *controller 1920*].

As per claim 19, Leung et al. discloses a plurality of target devices are accessed with a single base memory address [*a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module.* col.10, lines 21-25].

As per claim 20, Leung et al. discloses the plurality of target devices comprise a target group [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 21, Leung et al. discloses a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 22, Leung et al. discloses the transaction is a multicast read request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 23, Leung et al. discloses the transaction is a multicast write request [*multiple bank operations such as broadcast-write and interleaved-access*; col.5, lines 27-29; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

As per claim 25, Leung et al. discloses a computer system for multicast input/output transactions [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible. A memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; a processor, a communications bus coupled to the processor [*the two processors can reside on the same bus using the same memory module*; col.10, lines 40-42]; an initiator device coupled to the communications bus for issuing a multicast transaction, and a plurality of target devices coupled to the communications bus for executing the multicast transaction with

concurrent interleaved data responses [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible. A memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31].

As per claim 26, Leung et al. discloses the target devices comprise input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 27, Leung et al. discloses the target devices comprise disk array Controllers [Fig. 19].

As per claim 28, Leung et al. discloses the plurality of target devices comprise a target group, the target group addressable with a single base memory address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 29, Leung et al. discloses a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 30, Leung et al. discloses the multicast transaction is a multicast read request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 31, Leung et al. discloses the multicast transaction is a multicast write request [*multiple bank operations such as broadcast-write and interleaved-access*; col.5, lines 27-29; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. in view of Carmichael et al. (US 5,864,712).

As per claim 24, Leung et al. discloses the claimed invention as detailed above in the previous paragraphs. However, Leung does not specifically teach the

communications bus comprises a Peripheral Component Interconnect (PCI) bus as recited in the claim.

Carmichael discloses the communications bus comprises a Peripheral Component Interconnect (PCI) bus [*the bridge 36 may simply provide an extension of the processor's bus, or may buffer and extend the processor bus using an entirely different bus structure and protocol such as PCI*; col.6, lines 46-50] to provide an extension of the processor's bus and to buffer and extend the processor (col.6, lines 46-50).

Since the technology for implementing a data processing system using a PCI bus was well known in the art as evidenced by Carmichael, and since a PCI bus provides an extension of the processor's bus and to buffer and extend the processor, an artisan would have been motivated to implement a PCI bus in the data processing system of Leung. Thus it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Leung to include a PCI bus to provide an extension of the processor's bus and to buffer and extend the processor (col.6, lines 46-50) as taught by Carmichael.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Leung et al.	6,272,577
Leung et al.	6,754,746

Howard	5,950,218
Carmichael et al.	5,864,712

7. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 29, 2004

MC

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